IN THE CLAIMS

1. (Currently Amended) A synchronization circuit, comprising:

a local timestamp counter configured to generate a local timestamp value; and

a processing circuit ~~configured~~ to receive synchronization pulses and a predicted master timestamp value for a next synchronization pulse,

the processing circuit ~~identifying~~ to identify the local timestamp value at the next received synchronization pulse and ~~synchronizing~~ synchronize the local timestamp counter according to the identified local timestamp value and the predicted master timestamp value[[.]];

the processing circuit to receive an error message indicating that the predicted master timestamp value is not equal to an actual master timestamp value for the next synchronization pulse; and

the processing circuit to predict a new master timestamp value in response to the error message.

2. (Currently Amended) The synchronization circuit according to claim 1 wherein the processing circuit is located in a Cable Modem Termination System (CMTS) and receives the predicted master timestamp value from another CMTS.

3. (Currently Amended) The synchronization circuit according to claim 1 wherein the processing circuit receives the predicted master timestamp value asynchronously in Internet Protocol (IP) packets received over an IP connection.

4. (Currently Amended) The synchronization circuit according to claim 1 including a holding register configured to store the received predicted master timestamp value.

5. (Currently Amended) The synchronization circuit according to claim 2 [[1]] further comprising the processing circuitry to send the new predicted master timestamp value to the another CMTS ~~wherein the processor starts generating the master timestamp value and starts sending the master timestamp value to other synchronization circuits~~.

6. (Original) The synchronization circuit according to claim 1 wherein the synchronization pulse has a rate of somewhere between 8 Kilo Hertz and 1 Hertz.

7. (Currently Amended) The synchronization circuit according to claim 1 wherein the processing circuit identifies an error condition according to a number of times the local timestamp counter is synchronized with ~~the master~~ received timestamp values ~~value~~.

8. (Currently Amended) The synchronization circuit according to claim 1 including multiple line cards in a same Cable Modem Termination System (CMTS) chassis that each have local timestamp counters that are adjusted according to the received predicted master timestamp value and local timestamp values at the next received synchronization pulse.

9. (Original) The synchronization circuit according to claim 1 including a first CMTS including one or more line cards that are used for downstream channels and a second CMTS including one or more line cards that are used for upstream channels, cable modems receiving data on the downstream channels of the first CMTS and sending data on the upstream channels of the second CMTS.

10. (Currently Amended) A synchronization system, comprising:

a master synchronization circuit configured to:

identify a first master timestamp value associated with a first synchronization pulse and a second master timestamp value associated with a second synchronization pulse;

determine a difference between the first and second master timestamp values and an amount of time occurring between the first and second synchronization pulses;

predict the occurrence of a future synchronization pulse at a time equal to the amount of time multiplied by a predetermined amount;

calculate a future master timestamp value that corresponds to the future synchronization pulse by adding the second master timestamp value and the difference multiplied by the predetermined amount;

forward the calculated future master timestamp value to a slave synchronization circuit for synchronizing at the future synchronization pulse.

~~a master synchronization circuit configured to identify a reference timestamp value at a first one of multiple synchronization pulses and estimates a master timestamp~~

~~value for a later occurring one of the synchronization pulses according to the reference timestamp value, the master synchronization circuit forwarding the master timestamp value to a slave synchronization circuit for synchronizing at the later synchronization pulse.~~

11. (Currently Amended) The system according to claim 10 wherein the master synchronization circuit is further configured to:

identify an actual master timestamp value corresponding to the future synchronization pulse when the future synchronization pulse occurs;

determine whether a difference between the actual master timestamp value and the future master timestamp value is within a predetermined range; and

send an error message to the slave synchronization circuit when the difference between the actual master timestamp value and the future master timestamp value is not within a predetermined range.

~~derives master timestamp values for a subset of the synchronization pulses.~~

12. (Currently Amended) The system according to claim [[10]] 11 wherein the slave synchronization circuit is configured to calculate and forward new future master timestamp values in response to receiving the error message ~~wherein the master synchronization circuit sends the master timestamp value asynchronously to the slave synchronization circuit over an IP network.~~

13. (Currently Amended) The system according to claim [[10]] 12 including a first Cable Modem Termination Systems (CMTS) having a first chassis containing the master synchronization circuit and a second CMTS having a second separate chassis containing the slave synchronization circuit.

14. (Currently Amended) The system according to claim 13 including multiple lines cards in at least one of the first and second CMTS that includes multiple slave circuits each synchronized with the future master timestamp value at the future synchronization pulse when the difference between the actual master timestamp value and the future master timestamp value is within the predetermined range ~~at the later occurring synchronization pulse~~.

15. (Currently Amended) The system according to claim 10 wherein the slave synchronization circuit adjusts the received calculated future master timestamp value according to an amount of delay associated with receiving the synchronization pulses.

16. (Currently Amended) A method for synchronizing circuitry, comprising:

receiving [[a]] an extrapolated master timestamp value for an upcoming time reference over an asynchronous connection;

generating a local timestamp value;

comparing the local timestamp value at the upcoming time reference with the extrapolated master timestamp value; and

synchronizing the local timestamp value according to the comparison.

17. (Currently Amended) A method according to claim 16 including:

identifying a period between synchronization pulses;

extrapolating a time for a future synchronization pulse by adding one of the synchronization pulses to the period multiplied by a predetermined amount; and

extrapolating the master timestamp value by adding a master timestamp value for the one of the synchronization pulses and the predetermined amount multiplied by a difference between two previous master timestamp values.

~~determining a period for the time reference and then estimating the master timestamp value by adding the determined period to a timestamp counter value at a current pulse of the time reference.~~

18. (Currently Amended) A method according to claim 16 including receiving the extrapolated master timestamp value from a first cable modem termination system (CMTS) and using the extrapolated master timestamp value to synchronize a timing circuit in a second CMTS.

19. (Original) A method according to claim 16 including:

synchronizing the timing circuitry in a first Cable Modem Termination System (CMTS) with the timing circuitry in a second CMTS;

using the first CMTS to send data to cable modems; and

using the second CMTS to receive data from the same cable modems.

20. (Currently Amended) A method according to claim 16 further including:

receiving an error message indicating that the predicted master timestamp value is not equal to an actual master timestamp value for the next synchronization pulse;

predicting a new master timestamp value in response to the error message; and

sending the predicted new master timestamp value to a generation source of a message including the received extrapolated master timestamp value.

~~receiving the master timestamp value in a Internet Protocol (IP) message~~.

21. (New) The synchronization circuit of claim 1 wherein the predicted master timestamp value is equal to a sum of an actual master timestamp value for a previous synchronization pulse and a predetermined amount multiplied by a difference between two previous actual master timestamp values.

22. (New) The synchronization circuit of claim 21 wherein the predefined amount is equal to a quotient of a difference in time between the previous synchronization pulse and the next synchronization pulse divided by a period between synchronization pulses that corresponds to the two previous actual master timestamp values.